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ART UNIT	**PAPER NUMBER**
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/191,930	CHIANG ET AL.	
	Examin r	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *45-60,62-77 and 79-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *45-60,62-77 and 79-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The formal drawings were received on March 26, 2003. These drawings are acceptable.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 45-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 45 (Amended):

The limitation in the last four lines is indefinite because it is not clear *whether* the second dielectric material is deposited:

(1) **only** adjacent the third signal interconnect line wherein the third signal interconnect line is somehow located between the second power interconnect line and itself;

(2) adjacent the third signal interconnect line **and** between the second power interconnect line and the third signal interconnect line; *or*

(3) adjacent the third signal interconnect line **or** between the second power interconnect line and the third signal interconnect line.

In other words, this claim is indefinite because there seems to be at least three possible interpretations of the claim language. Examiner interprets the limitation as stated in "(2)".

Regarding Claims 46-49:

These claims are rejected as being indefinite because they depend from an indefinite claim (Claim 45).

Any further rejections of, or indications of the allowability of, Claims 45-49 are based on the Examiner's interpretation of Claim 45.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 45-49 and 63-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami (6,222,269) in view of Havemann (5,751,066) and Doo (4,153,988).

Regarding Claims 45 and 49:

Usami discloses (in Figs. 2A-3C and cols. 5-7) a method of forming an interconnect structure, comprising:

forming a first layer 4 of a first dielectric material on a substrate;

patterning the first layer (Fig. 2B);

depositing conductive material 13 over the patterned first layer;

planarizing the conductive material such that a plurality of interconnect lines 3 are formed including a first and a second "wide" interconnect lines (i.e., note the two interconnect lines "3" on the right side in Fig. 2D) and a third "thin" interconnect line (e.g., the third line

being the ***centrally located*** "thin" interconnect line "3" ***among the three "thin" interconnect lines "3"*** in Fig. 2D);

forming a mask layer 14 over the plurality of interconnect lines 3 and patterned first layer 4 (Fig. 3A);

patterning the mask layer 14 such that the first and second "wide" interconnect lines and a first portion of the patterned first layer 4 are covered, and the third "thin" interconnect line and a second portion of the patterned first layer 4 are uncovered;

removing the second portion of the patterned dielectric material of the first layer 4 from the uncovered portion (Fig. 3B); and

depositing a second layer 5 of a second dielectric material ***adjacent to the third "thin", centrally-located interconnect line "3" and*** between the second "wide" interconnect line(s) and third ***"thin", centrally-located interconnect line "3"***, the second dielectric material having a smaller dielectric constant than the first dielectric material (Fig. 3C and col. 6, lines 3-9).

Usami **lacks** specifying the plurality of interconnect lines includes power interconnect lines (first and second) and signal interconnect lines (third), however, it is important to note that Usami does not specify whether the interconnect lines "3" may or may not include a combination of power lines and signal lines. Note Usami specifies that a low-dielectric-constant material between signal lines reduces parasitic capacitance and crosstalk (see Usami, col. 8, lines 14-20). Havemann **teaches** a method of forming two different dielectric materials between a plurality of interconnect lines located on the same level of metallization, wherein the method comprises: forming a low-dielectric-constant material 34 (note Fig. 3B) between closely-spaced interconnect lines 18 in order to reduce unwanted capacitance between lines 18 (note col. 2, lines 35-37); and

forming a "higher" dielectric-constant material 26 between interconnect lines 16 where capacitance is not as critical (note abstract, line 3-5). Doo is **cited only** to show it was very well known in the art that problems associated with power lines (e.g., "driver noise", note col. 3, lines 51-55) can be reduced by increasing the capacitance of the power line (note col. 4, lines 13-16). The formula for capacitance is well known to any one in the art, and one of ordinary skill in the art would have known that, for a given separation between a pair of formed interconnect lines, the capacitance between the pair can be readily increased or decreased by forming a high-k or low-k dielectric (respectively) in between the pair of interconnect lines. In view of Havemann and Doo, it would have been obvious to one of ordinary skill in the art to modify Usami by utilizing the interconnect lines "3" for a combination of power lines and signal lines on the same level of metallization because the two dielectric materials ("4" and "5") can be readily utilized to increase capacitance between power lines and to decrease parasitic capacitance between signal lines. ***In other words, Usami and Havemann clearly indicate that signal lines will benefit from the low-k material wherein both Usami and Havemann perform dedicated process steps for the very purpose of locating low-k material between interconnect lines that are clearly intended for signal lines; and given the knowledge generally available regarding capacitance of signal lines and power lines (as shown by Doo), one of ordinary skill in the art would have readily recognized that the interconnect lines with the high-k material therebetween are ideal for power lines***. *Specifically regarding Claim 49*: The cited references are generally applicable to semiconductor devices; therefore, it would have been obvious to one of ordinary skill in the art to form a microelectronic device utilizing the method of Usami (in view of Havemann and Doo).

Regarding Claim 46:

Usami discloses the second dielectric material 5 comprises SOG having a dielectric constant (k=3) that is less than that of silicon dioxide (note col. 7, lines 27-36); and wherein the first dielectric material 4 comprises silicon dioxide.

Regarding Claims 47 and 48:

Usami discloses (in col. 11, lines 36-45) various materials suitable for the second dielectric material. Although Usami does not disclose that the first dielectric material may be of a material having a dielectric constant greater than that of silicon dioxide (i.e., barium strontium titinate "BST"), Havemann discloses various materials other than silicon dioxide may be incorporated as the high-dielectric-constant material (note materials for drawing element "26" in Table 1, cols. 5-6). The cited references disclose the claimed invention except for utilizing BST for the first dielectric material, however, it is noted that BST is/was a very well known high-dielectric-constant material that is/was commonly utilized in the art. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate BST as the high-k material, since it has been held to be within the general skill of a worker in the art to select a known material (i.e., BST) on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claims 63-65:

Usami discloses a method of forming an interconnect structure, comprising:

forming on a substrate a first intralayer dielectric 4 and a first plurality of interconnect lines 3 disposed within the first intralayer dielectric 4 (Fig. 2D);

removing a portion of the first intralayer dielectric 4 (Fig. 3B); and

forming a second intralayer dielectric 5 on the substrate where the first intralayer dielectric was removed (Fig. 3C), wherein a dielectric constant of the first intralayer dielectric is different from a dielectric constant of the second intralayer dielectric (the first dielectric is a relatively high-k material and the second dielectric is a low-k material).

Usami **lacks** the following: (1) forming a second plurality of interconnect lines in the second interlayer dielectric, and (2) specifying whether the interconnect lines 3 may or may not include signal lines and power lines. In regards to lacked limitation (1), it is noted Usami discloses forming all conductive lines simultaneously, wherein a plurality of interconnect lines will exist within the second interlayer dielectric layer when said second interlayer dielectric layer is formed. Havemann **teaches** (in Figs. 2A-3B) a method of forming two different dielectric materials between interconnect layer on the same level of metallization, wherein the method can include forming a first plurality of interconnect lines 16 with a first dielectric material between the lines 16, and then forming a second plurality of interconnect lines 18 with a second dielectric material between the lines 18. It is important to note Havemann also teaches (in Figs. 5A-6E) the interconnect lines 16 and 18 may be formed simultaneously instead of forming two pluralities that would require at least two masking/patterning steps, in other words, in view of Havemann, one of ordinary skill in the art would have realized that the interconnect lines of Usami could also be formed in two pluralities, wherein forming two pluralities would require the utilization of at least two masking/patterning steps. In regards to lacked limitation (2), Doo is **cited only** to show that one of ordinary skill in the art would have realized that the interconnect lines of Usami (or Havemann) are ideal for power lines and signal lines. Doo discloses the well-known problems associated with signal lines and power lines (note col. 3, lines 28-55), wherein

problems such as signal propagation delay can be reduced by utilizing a low-dielectric-constant material and problems associated with power lines can be reduced by increasing capacitance of the power lines (note col. 4, lines 13-16), in other words, it was well known in the art to utilize a low-dielectric-constant material between signal lines and to increase the capacitance of power lines in order to effectively decouple noise from the power lines, wherein utilizing a "higher" dielectric-constant material between the power lines is a relatively quick and easy way to increase the capacitance between the power lines. It would have been an obvious matter of design choice for one of ordinary skill in the art to modify Usami by (*i*) forming two pluralities of interconnect lines instead of simultaneously forming all interconnect lines and (*ii*) specifying that the interconnect lines comprise signal lines and power lines because of the following reasons: (*1*) Havemann teaches that either a simultaneous process or two separate patterning processes may be utilized to form interconnect lines on the same level of metallization, and one of ordinary skill in the art would have realized that Usami can also be modified by forming the interconnect lines utilizing two separate patterning processes, wherein one would have realized that two separate patterning processes would increase process time and complexity without any apparent significant benefits, however, one could obviously choose to do so; and (*2*) the methods disclosed by Usami and Havemann are ideal for acquiring a combination of signal lines and power lines on the same level of metallization, since it was well known in the art (as shown by Doo) that it is desirable to form a low-dielectric-constant material between adjacent signal lines and that it is desirable to increase the capacitance of power lines (e.g., by incorporating a "higher" dielectric-constant material between adjacent power lines).

Regarding Claim 66:

This claims is similar to Claim 48, therefore, it is held obvious over the cited references with reasoning similar to that applied to Claim 48.

Regarding Claim 67:

In general, the instant claim contains limitations for forming interconnect lines by a damascene process, and although Usami lacks forming a second plurality of interconnect lines, Havemann teaches that interconnect lines on the same level of metallization can be formed by utilizing a simultaneous process or plural processes. The instant claim is held obvious over the cited references because of the following reasons: **(a)** Usami discloses a damascene process, in Figs. 2A-2D, wherein the plurality of conductive lines 3 are formed by etching trenches in the first intralayer dielectric 4, depositing a conductive material 13, and polishing the conductive material such that the conductive material is substantially removed except for that which is in the trenches; **(b)** Usami discloses forming all conductive lines simultaneously using a single damascene process instead of, for example, forming the conductive lines utilizing two separate damascene processes; **(c)** one of ordinary skill in the art would have readily recognized that Usami could be modified, if so desired, by forming several "pluralities" of conductive lines utilizing two or more damascene processes, especially since Havemann teaches interconnect lines on the same level of metallization, having two different dielectrics therebetween, can be formed utilizing a simultaneous process or plural processes; **(d)** forming the conductive lines in several "pluralities" would increase process time and complexity without significant benefits, however, one could obviously choose to do so if time and cost are not an issue; therefore, if one chooses to form the conductive lines (of Usami) in several "pluralities" (i.e., in a first and second

plurality of lines), then it would have been obvious to utilized the process steps in "**(a)**" when forming each of the several "pluralities" of conductive lines.

Regarding Claim 69:

Usami discloses a method of forming an interconnect structure comprising:

(A) forming a first dielectric layer 4 on a substrate;

(B) forming a plurality of interconnect lines 3 in the first dielectric layer 4 (Fig. 2D);

(C) removing a portion of the first dielectric layer 4 (Fig. 3B); and

(D) forming a second dielectric layer 5 on the substrate where the portion of the first dielectric layer was removed, wherein the plurality of interconnect lines 3 are positioned in the first and second dielectric layers.

Usami **lacks** performing step "(B)" after step "(D)" and specifying that the interconnection lines 3 comprise a plurality signal lines and a power line. In view of Havemann and Doo, it would have been an obvious matter of design choice to specify that interconnect lines 3 comprise a combination of signal lines and a power line, since Usami's disclosure is ideal for such a specification (see above, Regarding Claims 45 and 63, for detailed reasoning for such a specification/utilization of the interconnect lines 3). Only the lacked limitation of performing step "(B)" after step "(D)" will be currently addressed in detail, in other words, in reference to the instant claim, Usami **lacks** forming a plurality of interconnect lines simultaneously in the first and second dielectric layers. In general, Usami discloses the inventive aspect of Applicants' disclosure, i.e., Usami discloses forming an interconnect structure comprising two different dielectric layers having different dielectric constants formed between a plurality of interconnect lines such that the dielectric layers and the interconnect lines are on the same level of

metallization, wherein incorporating the two dielectric layers can at least prevent crosstalk (and reduce parasitic capacitance) between signal lines having the "lower" dielectric constant of the two dielectric layers. Although the instant claim recites a different sequence than that disclosed by Usami, the instant claim is held obvious because of the following reasons: Usami discloses the general conditions of the instant claim; the instant claimed process sequence may require more processing steps than Usami's disclosed sequence, i.e., the first dielectric will need to be etched twice in both sequences, however, in the instant claimed sequence, it may not be possible to simultaneously etch openings in both dielectric layers using the same mask or etching chemistry, since the dielectric layers would be formed of different materials; given Usami's disclosure, one of ordinary skill in the art would have readily recognized that forming all the interconnecting lines after forming the second dielectric layer would be a matter of design choice, since such a choice would not reduce the number of process steps; therefore, it would have been an obvious matter of design choice for one of ordinary skill in the art to modify Usami by performing step "(B)" after step "(D)", since there seems to be no significant benefit for choosing such a modification.

Regarding Claims 70 and 72:

Usami discloses the dielectric constant of the first dielectric is different than that of the second dielectric, wherein the second dielectric comprises low-k material and the first dielectric comprises a relatively high-k material (i.e., relatively high in comparison to the low-k, first dielectric).

Regarding Claim 71:

The instant claim, similar to Claim 26, contains limitations for forming the interconnect lines using a damascene process. With similar reasoning applied to claim 26 above, the instant claim is held obvious over the cited references, i.e., a damascene process as instantly claim was well known and used in the art.

Regarding Claims 68 and 73:

The cited references are generally applicable to semiconductor devices; therefore, it would have been obvious to one of ordinary skill in the art to form a microelectronic device utilizing the method of Usami (in view of Havemann and Doo).

6. Claims 50-60, 62, 74-77, and 79-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann (5,751,066) in view of Doo (4,153,988).

Regarding Claims 50, 74-77, 79, 82, and 83:

Havemann discloses a method of forming an interconnect structure, comprising:

forming a first layer of a conductive material (15, 17) on a substrate 12 (Fig. 5A);

forming a first pair of interconnect lines 16 and a second pair of interconnect lines 18 (Fig. 5C);

depositing a first dielectric material 26 over and between the first pair and the second pair (Fig. 5D);

forming a masking layer 50 over the first pair and the second pair and first dielectric material (Fig. 5E and col. 8, lines 26-32);

patterning the mask layer 50 such that one portion of the dielectric material 26 between one pair is covered and another pair is uncovered (Fig. 5F);

removing the portion of the dielectric material that is uncovered (Fig. 6A);

removing the patterned mask layer (Fig. 6B); and

depositing a second dielectric material 34 having a different dielectric constant than a dielectric constant of the first dielectric material ***26 where the portion of the dilectric material was removed*** (Note Table 1; Fig. 6C; and col. 8, lines 36-37), wherein the second material comprises a low-k material and the first material comprises a relatively high-k material (i.e., relatively high in comparison to the second material).

Havemann **lacks** specifically disclosing that lines "16" are for power distribution and that lines "18" are for carrying signals. Doo is **cited only** to show that one of ordinary skill in the art would have readily recognized that the interconnect lines "16" and "18" (of Havemann) are ideal for power lines and signal lines, respectively. Doo discloses the well-known problems associated with signal lines and power lines (note col. 3, lines 28-55), wherein problems such as signal propagation delay can be reduced by utilizing a low-dielectric-constant material and problems associated with power lines can be reduced by increasing capacitance of the power lines (note col. 4, lines 13-16), in other words, it was well known in the art to utilize a low-dielectric-constant material between signal lines and to increase the capacitance of power lines in order to effectively decouple noise from the power lines, wherein utilizing a "higher" dielectric-constant material between the power lines is a relatively quick and easy way to increase the capacitance between the power lines. It would have been obvious to one of ordinary skill in the art to modify Havemann by specifying that interconnect lines "16" and "18"are utilized to

distribute power and carry signals, respectively, because the interconnect structure formed by Havemann is ideal for such a utilization. *Specifically regarding Claim 77:* Havemann (in view of Doo) discloses the general conditions of the claimed invention except for utilizing BST for the high-dielectric-constant material, however, it is noted that BST is/was a very well known high-dielectric-constant material that is/was commonly utilized in the art. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate BST as the high-k material, since it has been held to be within the general skill of a worker in the art to select a known material (i.e., BST) on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claim 56:

Havemann discloses a method of making in-plane decoupling capacitors, comprising:

forming a first plurality of conductive lines 16 on an insulating substrate 12, the first plurality of conductive lines having a first dielectric 26 therebetween (Figs. 1A-2B); and

forming a second plurality of conductive lines 18 on the insulating substrate 12, the second plurality of conductive lines having a second dielectric material 34 therebetween (Figs.2D-3B);

wherein the first dielectric constant is greater than a dielectric constant of the second dielectric.

Havemann **lacks** specifically disclosing that conducive lines "16" are power lines and that conductive lines "18" are signal lines. Doo is **cited only** to show that one of ordinary skill in the art would have readily recognized that the interconnect lines "16" and "18" (of Havemann) are ideal for power lines and signal lines, respectively. With similar reason applied above, the

instant claim is held obvious over the cited references (See above, *Regarding Claims 50 and 74* for detailed reasoning).

Regarding Claims 51-54 and 57-60:

These claims generally contain limitations for a relationship between the dielectric constants of the first and second dielectric materials. Havemann discloses various materials can be utilized for the first and second dielectric materials "26" and "34" (note Table 1, cols. 5-6), wherein materials listed in Table 1 can be readily selected to arrive at the limitations of the current claims. It would have been an obvious matter of design choice for one of ordinary skill in the art to utilized first and second dielectric materials have dielectric constants as specified in the current claims because Havemann discloses a list of materials wherein one can readily choose materials having specific dielectric constants according to design needs. *Specifically regarding Claims 60:* Havemann (in view of Doo) discloses the general conditions of the claimed invention except for utilizing BST for the high-dielectric-constant material, however, it is noted that BST is/was a very well known high-dielectric-constant material that is/was commonly utilized in the art. Therefore, it would have been obvious to one of ordinary skill in the art to incorporate BST as the high-k material, since it has been held to be within the general skill of a worker in the art to select a known material (i.e., BST) on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding Claims 55, 62, and 84:

Havemann (in view of Doo) is generally applicable to semiconductor devices; therefore, it would have been obvious to one of ordinary skill in the art to form a microelectronic device utilizing the method of Havemann (in view of Doo).

Regarding Claims 80 and 81:

These claims contain limitations for forming the low-dielectric-constant material between the signal lines before forming the "higher" dielectric-constant material between the power lines. Given Havemann, one of ordinary skill in the art could have modified the process sequence shown in Figs. 5C-6C with relative ease by performing the following modifications: replacing material "26" with material "34" in the process shown in Fig. 5D; forming/patterning the mask "50" to cover lines "18" instead of lines "16"(in the process shown in Fig. 5E); removing material "34" not covered by mask "50", i.e., removing material "34" over lines "16" (in the process shown in Fig. 6A); removing the mask "50" (in the process shown in Fig. 6B); and forming material "26" over lines "16" wherein the material "26" would overlap material "34" in the process shown in Fig. 6C. Such a modification would not have required extensive experimentation or research because, in general, the modification would be based on design choice, i.e., based on choosing first to form the low-dielectric-constant material "34" and then patterning the mask "50" accordingly, therefore, the instant claims are held as obvious design choice modifications (of Havemann) that would have been relatively easily performed by one of ordinary skill in the art.

Status of the Claims

7. Claims 61 and 78 have been canceled.

8. Claims 45-60, 62-77, and 79-84 are pending.

Remarks

9. Applicants' remarks/arguments have been carefully reviewed and considered but they are not persuasive. In general, Applicants remarks/arguments are similar to those presented in Paper No. 17 (i.e., in the "preliminary amendment" filed with the RCE on November 14, 2002). The amendments to the claims do not patentably distinguish the current invention over the applied prior art. In regards to Applicants' remarks/arguments, the examiner generally maintains his position, which was explained in detail in the previous Office action (i.e., Paper No. 18), and for brevity, the detailed position presented in the previous Office action will not be repeated in its entirety; however, a few critical points will be repeated in an attempt to further clarify the Examiner's position.

Initially, attention is directed to page 13 (last paragraph) of Applicants' remarks (Paper No. 20), wherein the overlying basis of Applicants' arguments seems to be summarized, i.e., Applicants submit that it is not known to reduce drive noise between power lines and reduce parasitic capacitance between signal lines in a given interconnect level by using different materials between power lines than between the signal lines. Applicants further submit that the Examiner has not documented that this knowledge is available to one of ordinary skill in the art. It is emphasized that Applicant's admit (in the specification, page 6, lines 11-21) that the concept of capacitance between interconnect lines in integrated circuits is well-known, furthermore, Applicants acknowledge that interconnect lines on integrated circuits are generally used for the distribution of power **and** signals. If the concept of capacitance between interconnect lines is well-known (as admitted by Applicant) and it is also well-known (as shown by Doo) that it is desirable to increase capacitance of power lines and to decrease capacitance

between signal lines; then the knowledge available to one of ordinary skill in the art would clearly indicate that, in Usami and Havemann, it would be desirable to utilize the interconnect lines having low-k material in between (i.e., the "low-k interconnect lines") for signal lines and the interconnect lines having high-k material in between (i.e., the "high-k interconnect lines") for power lines, especially since Applicants admit that it well known in the art that interconnections are generally used for the distribution of power **and** signals.

The current invention is held obvious over the cited reference primarily because Usami and/or Havemann disclose all significant aspects of the current claims, and the only significant modification to Usami and/or Havemann, necessary to arrive at the current invention, is for one of ordinary skill in the art to realized that the interconnect lines (in Usami and/or Havemann) can be used for distribution of power and signals. In other words, no significant modification of Usami and/or Havemann is necessary to arrive at the current invention, but rather, one only needs to realize that the interconnect lines can function as power lines and signal lines. Since Applicants acknowledge it is well known in the art that interconnect lines are generally used to distribute power **and** signals, one of ordinary skill in the art would have clearly realized that the interconnect lines of Usami and/or Havemann can be used for power lines **and** signal lines; furthermore, Applicants admit that the concept of capacitance is also very well known such that one of ordinary skill in the art would have clearly realized that the "high-k interconnect lines" are ideal for power lines, especially since both Usami and Havemann perform intricate/dedicated process steps for the very purpose of forming "low-k interconnect lines" and "high-k interconnect lines" on the same level of metallization, wherein the "low-k interconnect lines" are clearly for signal lines.

Summarizing, the current claims includes a modification that distinguishes over Usami and Havemann by specifying that the interconnect lines distribute power as well as signals; however, the modification is not considered to be patentable over Usami and/or Havemann because one of ordinary skill in the art, given the knowledge generally available, would have clearly realized that the interconnect lines (of Usami and/or Havemann) can be used for power lines **and** signal lines.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 703-306-5986.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lex Malsawma

June 1, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800